Evolution of Intel Microprocessors: 1971 to 2007

Family	Trade Name (Code Name for Future Chips)	Clock Frequency in MegaHertz**	Millions of Instructions per Second	Date of Introduction	Number of Transistors	Design Rule (Pixel Size)	Address Bus Bits
81186	Projected Roadmap	24,000.0 MHz	25,000.00+MIPS	2007	1 billion	0.045 micron	64 bit
81086	(Northwood)	3,000.0 MHz	TBA	2003	TBA	0.09 micron	64 bit
80986	Itanium 3 (Madison)	1,500.0 MHz	9,000.00 MIPS	2003H2	TBA	0.09 micron	64 bit
80886	Itanium 2 (Deerfield)	*** TBA	TBA	2003	TBA	0.09 micron	64 bit
80886	Itanium 2 (McKinley)	1,000.0 MHz	6,000.00 MIPS	July 8, 2002	291 million	0.18 micron	64 bit
80786	Itanium 1 (Merced)	800.0 MHz	4,800.00 MIPS	May 29, 2001	25.4 / 295 M	0.18 micron	64 bit
80687	Pentium 5 (Prescott)	3,200.0 MHz	3,200.00 MIPS	2003Q2	55 million	0.09 micron	32 bit
80686	Pentium 4	2,200.0 MHz	*2,200.00 MIPS	January 6, 2002	55 million	0.13 micron	32 bit
80686	Pentium 4 (Willamette	1,500.0 MHz	*1,500.00 MIPS	November 20, 2000	42 million	0.18 micron	32 bit
80686	Pentium III	1,000.0 MHz	*1,000.00 MIPS	March 1, 2000	28.1 million	0.18 micron	32 bit
80686	P III Xeon	733.0 MHz	*733.00 MIPS	October 25, 1999	28.1 million	0.18 micron	32 bit
80686	Mobile P II	400.0 MHz	*400.00 MIPS	June 14, 1999	27.4 million	0.18 micron	32 bit
80686	P III Xeon	550.0 MHz	*550.00 MIPS	March 17, 1999	9.5 million	0.25 micron	32 bit
80686	Pentium III	500.0 MHz	*500.00 MIPS	February 26, 1999	9.5 million	0.25 micron	32 bit
80686	P II Xeon	400.0 MHz	*400.00 MIPS	June 29, 1998	7.5 million	0.25 micron	32 bit
80686	Pentium II	333.0 MHz	*333.00 MIPS	January 26, 1998	7.5 million	0.25 micron	32 bit
80686	Pentium II	300.0 MHz	*300.00 MIPS	May 7, 1997	7.5 million	0.35 micron	32 bit
80586	Pentium Pro	200.0 MHz	*200.00 MIPS	November 1, 1995	5.5 million	0.35 micron	32 bit
90586	Pentium	133.0 MHz	*133.00 MIPS	June 1995	3.3 million	0.35 micron	32 bit
80586	Pentium	90.0 MHz	*90.00 MIPS	March 7, 1994	3.2 million	0.60 micron	32 bit
80586	Pentium	60.0 MHz	*60.00 MIPS	March 22, 1993	3.1 million	0.80 micron	32 bit
80486	80486 DX2	50.0 MHz	*50.00 MIPS	March 3, 1992	1.2 million	0.80 micron	32 bit
80486	486 DX	25.0 MHz	20.00 MIPS	April 10, 1989	1.2 million	1.00 micron	32 bit
80386	386 DX	16.0 MHz	5.00 MIPS	October 17, 1985	275,000	1.50 micron	16 bit
80286	80286	6.0 MHz	0.90 MIPS	February 1982	134,000	1.50 micron	16 bit
8086	8086	5.0 MHz	0.33 MIPS	June 8, 1978	29,000	3.00 micron	16 bit
8080	8080	2.0 MHz	0.64 MIPS	April 1974	4,500	6.00 micron	8 bit
8008	8008	.2 MHz	0.06 MIPS	April 1972	3,500	10.00 micron	8 bit
4004	4004	.1 MHz	0.06 MIPS	November 15, 1971	2,300	10.00 micron	4 bit

* Approximately one instruction per processor clock cycle // + /starting with Itanium, the chips have multiple floating point processors per chip

** 1 KHz (KiloHertz) = 1 thousand cycles per second; 1 MegaHertz = 1 thousand KiloHertz; 100 KHz = .1 MHz,
1 GHz (GigaHertz) = 1 billion cycles per second; 1 GigaHertz = 1 thousand MegaHertz / 1 micron = 1 millionth of a meter / 1 nanometer = 1 billionth of a meter

TBA To be announced *** Deerfield is a low cost blade version of the Itanium 2.

http://www.esc-ca.com/processors/intel/future.htm (one source of data for future microprocessors)

http://www.Intel.com/pressroom.htm (source of data for released microprocessors)

1.00	microns =	1,000 nanometers
0.25	microns =	250 nanometers
0.13	microns =	130 nanometers
0.09	microns =	90 nanometers
0.045	microns =	45 nanometers

MHz (MegaHertz) (Millions of processor cycles per second) The number of times the processor goes through one cycle. The start of a processor cycle is determined by a pulse (tick) from the processor's clock.

GHz (GigaHertz) (Billions of processors cycles per second). 1 thousand MHz = 1 GHz

MIPS: (Millions of Instructions per Second) with the introduction of the 80486 DX2, parallel instruction execution increased the number of instructions executed per processor cycle to approximately one instruction per cycle. Parallel instruction execution requires many more transistors, so the increase in the number of transistors has increased the number of instructions that can be executed per second faster than the clock cycle speed has increased. A larger transistor budget allows the addition of specialized instructions, which increase the microprocessor's speed in processing specialized information such as graphics by increasing the amount of information processed per instruction.

+Multiprocessors on the chip produce more than one instruction per clock cycle.

GIPS (GigaInstructions per Second) Billions of instructions per second. 1 thousand MIPS = 1 GIP

Design Rule: because the wires and components, including transistors, on chips are drawn photographically, the pixel size of the imaging process determines the width of the wires and the size of the transistors. The size of the transistors determines how many will fit on a chip of a given size. (The optimal size of a chip depends on the chip manufacturing processes. In general, chip size increases slowly over time.) The smaller the transistors, the more will fit on the chip, determining the chip's transistor budget. The size of the transistors also determines the transistor's switching speed. Smaller transistors switch faster. One micron is one one-millionth of a meter or about 40 millionths of one inch. Finally, the power required to switch smaller transistors is less, so smaller pixels in the design rules allow the batteries in laptop computers to last longer.

Number of Transistors: The number of transistors increases as the square of decrease in design rule size. Each reduction in design rule size is chosen to about double the number of available transistors (the transistor budget). [For example: (.25micron / .18 micron) x (.25 / .18) = 2.] The gradual increase in die size (the size of the chip) also increases the number of transistors. The Itanium chip has 30 million processor transistors and 300 million memory cache transistors

Address Bus Bits: The address bus width in bits is based on the microprocessor chip family. (In the later chips of the 80686 family, some changes have been made to make more memory addressable under special circumstances, by using 36 bits to address 16 times as much memory as is possible with 32 address bits, but the generalized addressing structure is still 32 bits.) Each time a bit is added to the address bus width, the amount of memory (RAM: Random Access Memory) that can be addressed is doubled. 4 bit addresses allow the addressing of 16 bytes of memory (and extra work is necessary to address 256 bytes of memory). 8 bits allow the addressing of 256 bytes of memory (and extra work is necessary to address 65,536 bytes of memory). 16 bits can address 65,536 bytes of memory. 32 bits can address 4,294,967,296 bytes of memory (about 4 billion bytes). As memory prices drop, it becomes necessary to address over 4 billion bytes of memory. The 80786 family, (the Itanium) debuted May 29, 2001. It has a 64 bit address bus and will be able to address over 16 billion billion (16 quintillion) bytes of memory.

See also: http://www.intel.com/intel/intelis/museum/ Intel's history of the microprocessor.